LISTING OF CLAIMS

1-46. (Cancelled).

47. (Previously Presented) A memory device, comprising:

a first conductive stud and a second conductive stud;

an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive stud; and

an insulating sidewall separating said interconnect line from said second conductive stud.

48. (Previously Presented) The memory device of claim 47, wherein said first and second conductive studs comprise epitaxial silicon.

49. (Original) The memory device of claim 48, wherein said first conductive epitaxial silicon stud has a silicide cap and said second conductive epitaxial silicon stud does not have a silicide cap.

50. (Original) The memory device of claim 48, wherein said interconnect line is a bit line.

51. (Previously Presented) The memory device of claim 48, wherein said insulating sidewall extends within a contact opening to said second conductive epitaxial silicon stud, wherein said contact opening is through an insulating layer which is over and around said interconnect line.

52. (Previously Presented) The memory device of claim 51, comprising a conductive plug to said second conductive epitaxial silicon stud and within said insulating sidewalls.

53. (Original) The memory device of claim 52, wherein said conductive plug forms a capacitor bottom electrode.

54. (Original) The memory device of claim 48, wherein said first and second conductive epitaxial silicon studs are connected to respective source and drain regions of a transistor.

55. (Original) The memory device of claim 54, wherein said first conductive epitaxial silicon stud is between wordline gates and said second conductive epitaxial silicon stud is between a wordline gate and an isolation gate.

56. (Original) The memory device of claim 54, wherein said transistor is an access transistor of a memory cell.

57. (Original) The memory device of claim 50, wherein said conductive plug comprises epitaxial silicon.

58. (Previously Presented) A DRAM cell structure, comprising:

an access transistor with source and drain areas;

a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud each in contact with a respective one of said source and drain areas of said access transistor;

a bit line over and in electrical contact with said first conductive epitaxial silicon stud, wherein at least a portion of said bit line overlays a portion of said second conductive epitaxial silicon stud; and

an insulating sidewall structure separating said bit line from said second conductive epitaxial silicon stud.

59. (Original) The DRAM cell structure of claim 58, wherein said first conductive epitaxial silicon stud has a silicide cap and said second conductive epitaxial silicon stud does not have a silicide cap.

60. (Previously Presented) The DRAM cell structure of claim 58, wherein said insulating sidewall structure is within a contact opening to said second conductive epitaxial silicon stud, wherein said contact opening extends through an insulating layer over and around said bit line.

61. (Original) The DRAM cell structure of claim 60, comprising a conductive plug within said insulating sidewall and in contact with said second conductive epitaxial silicon stud.

62. (Original) The memory device of claim 61, wherein said conductive plug is a capacitor bottom electrode.

63. (Original) The DRAM cell structure of claim 61, wherein said conductive plug is epitaxial silicon.

64. (Original) A DRAM cell structure, comprising:

at least one wordline gate and at least one isolation gate on a semiconductor substrate;

an insulating layer on and around said at least one wordline gate and said at least one isolation gate;

at least one first epitaxial silicon stud with a silicide cap and at least one second epitaxial silicon stud without a silicide cap, each said stud in contact with a respective source and drain region of said at least one wordline gate;

at least one bit line over and in electrical contact with said at least one first epitaxial silicon stud and partially overlying said at least one second epitaxial silicon stud, but electrically isolated therefrom by an insulating sidewall; and

a conductive plug within said insulating sidewall and in electrical contact with said second epitaxial silicon stud.

65. (Previously Presented) The DRAM cell structure of claim 64, wherein said first epitaxial silicon stud is between said at least one wordline gate and a second wordline gate, and said second epitaxial silicon stud is between said at least one wordline gate and said at least one isolation gate.

66. (Original) The DRAM cell structure of claim 64, wherein said second epitaxial silicon stud is a capacitor stud.

67. (Original) The DRAM cell structure of claim 64, wherein said conductive plug forms a capacitor bottom electrode.

68. (Original) The DRAM cell structure of claim 64, wherein said conductive plug is epitaxial silicon.

69. (Previously Presented) A processor-based system, comprising:

a processor; and

a memory circuit connected to said processor, wherein said memory circuit includes a memory device comprising:

a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud;

an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive epitaxial silicon stud; and

an insulating sidewall structure separating said interconnect line from said second conductive epitaxial silicon stud.

70. (Original) The processor-based system of claim 69, wherein said first conductive epitaxial silicon stud has a silicide cap and said second conductive epitaxial silicon stud does not have a silicide cap.

71. (Original) The processor-based system of claim 69, wherein said interconnect line is a bit line.

72. (Previously Presented) The processor-based system of claim 69, wherein said insulating sidewall structure is within a contact opening to said second conductive

epitaxial silicon stud, wherein said contact opening is through an insulating layer which is over and around said interconnect line.

73. (Original) The processor-based system of claim 72, comprising a conductive plug to said second conductive epitaxial silicon stud within said insulating sidewalls.

74. (Original) The processor-based system of claim 73, wherein said conductive plug forms a capacitor bottom electrode.

75. (Original) The processor-based system of claim 71, wherein said first and second conductive epitaxial silicon studs are connected to respective source and drain regions of a transistor.

76. (Original) The processor-based system of claim 75, wherein said first conductive epitaxial silicon stud is between wordline gates and said second conductive epitaxial silicon stud is between a wordline gate and an isolation gate.

77. (Original) The processor-based system of claim 75, wherein said transistor is an access transistor of a memory cell.

78. (Original) The processor-based system of claim 73, wherein said conductive plug comprises epitaxial silicon.